ABSTRACT OF THE DISCLOSURE

A shift register receives a quantization difference signal separated into a mantissa part and an exponent part and bit-develops the mantissa part. A shift arithmetic operation control circuit bit-shifts the bit-developed mantissa part in accordance with a value of the exponent part. An overflow detection bit is added to the MSB of the shift register and detects the overflow of the bit-shifted mantissa part. When the overflow of the mantissa part is detected, a selector replaces the bit-developed mantissa part with a predetermined upper limit value and outputs it as a prediction signal. When the overflow is not detected, the selector outputs the bit-developed mantissa part as a prediction signal. An ADPCM decoder having high audio quality is provided by simple processes and construction.